New approach to GaAs MESFET Analog Frequency dividers with low threshold input power and high conversion gain

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ABSTRACT

A new approach to frequency dividers is proposed based on the nonlinear feedback control of MESFET in forced oscillation mode. The input signal is used to control the FET gain, imposing oscillation conditions.

Firstly, this approach is tested by time domain simulation. An experimental MESFET analog frequency divider is then achieved.

1-INTRODUCTION

Analog frequency dividers are essential circuits for phase-locked loops and FM communication system[1].

Many concepts have been proposed to achieve frequency division. Miller's representation [2] is one of the most often used [3][4][5][6]. Unfortunately, this method is not sufficient when a single component performs many interactive operations and several electronic functions. Furthermore, frequency representations are difficult to use when the circuit is strongly nonlinear and unstable. Other authors have proposed a small signal approach [7] to design frequency dividers. But some circuit characteristics, like loop gain, depend on the applied signal level and cannot be predicted by these methods.

Our original approach is based on the nonlinear feedback control of MESFET in forced oscillation mode. The input signal is used to control transistor gain, imposing oscillation conditions. The advantage provided by this approach, essentially lies in the possibility of using a time domain representation which is the natural for nonlinear elements.

The FET is biased near pinch-off. The input signal relies on the autopolarisation phenomenon to increase the FET dc transconductance and loop gain at subharmonic oscillation. Concurrently, the transmission of the informative signal has been verified.

Simulation and measurement of FET autopolarisation phenomenon are performed and its effect on gain are shown. The original concept is confirmed by the temporal simulation using commercial software. Then, an experimental 8GHz frequency divider by 2 is achieved with high maximum gain (typically 10dB) and low threshold input power (-4dBm).

This concept can be applied to other transistors to achieve frequency dividers by any ratio.

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2-OPERATION PRINCIPLE

Fig.1 shows the block diagram allowing the use of our new approach to frequency division. The FET is the nonlinear element represented by its nonlinear gain N(er) as a function of its input value(er).

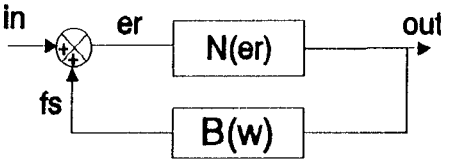

Fig.1 frequency divider black box diagram

The total gain is

$$G = \frac{V_{out}}{V_{in}} = \frac{N(e_r)}{1-N(e_r).B(w)}$$

To avoid free oscillations the following condition must be satisfied :

$$B(w)N(0) << 1$$

The FET, biased in pinch-off region, allows this condition to be verified. The forced subharmonic oscillation conditions at the pulsation $\frac{w}{2}$ are

$$|N(er).B(\frac{w}{2})| > 1 \text{ and } Arg[(N(er).B(\frac{w}{2})] = 2.k.\pi$$

The first condition is obtained by increasing the FET gain thanks to the autopolarisation of its drain current by the input signal. The second condition requires adjusting phase in the loop.

2-ANALYSIS AND SIMULATION

The dc drain current changes with the input signal er(t) at its gate, when the MESFET is biased in the pinch-off region. This current can be calculated using Fourier's transform, then the drain current is approximated by:

$$Ids(t) = Idss.(1 - \frac{Vgs}{Vt})^2 \quad \text{if} \quad Vgs > Vt$$

Where Idss is the drain saturation current and Vt is the pinch-off voltage value.

The FET input signal may be writen as

$$V_{er}(t) = V_{in}(t) + V_{fs}(t)$$

$$V_{er}(t) = V_{in}.\sin(2.\pi.F.t) + V_{fs}.\sin(2.\pi.\frac{F}{2}.t)$$

Where V_{fs} is a small signal representing the beginning of an oscillation at frequency $\frac{F}{2}$ and V_{in} is input signal.

The dc drain current Ids_0 and the transconductance gm_0 are given respectively by

$$Ids_0 = \frac{1}{T}\int_0^T Ids(t)dt = \frac{Idss}{4}.(\frac{V_{in}^2+V_{fs}^2}{Vt^2}) \qquad (1)$$

$$gm_0 = \frac{1}{T}\int_0^T \frac{\delta Ids(t)}{\delta Vgs}dt = Idss.\frac{V_{in}+V_{fs}}{Vt^2} \qquad (2)$$

Equations (1) and (2) show that Ids_0 and gm_0 increase with the input value e. Also, the FET gain, increases according to the dc transconductance value.

The FET model[8] used for simulation is that of TAJIMA shown in Fig.2. The only nonlinearity of this model is the drain current.

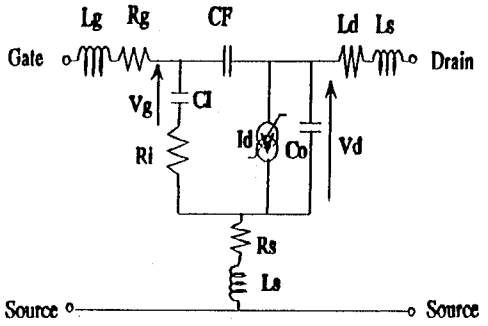

Fig.2 Nonlinear MESFET model

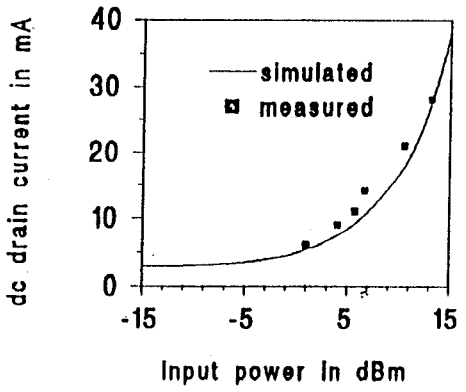

Fig.3 dc drain current Ids_0 versus Input power Pin

Fig.3 shows dc drain current simulated as a function of the input's power FET.

The FET gain N(er) at the beginning of the $\frac{F}{2}$ frequency oscillation is simulated. This gain increases with the input power as shown in Fig.4. The $\frac{F}{2}$ frequency oscillation can be kept up when N(er) is higher than the loop loss. When this loss is about 5dB the predicted input power threshold is -5dBm.

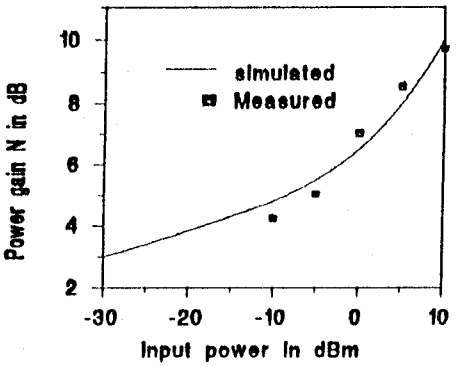

fig.4 FET gain N of low ($\frac{F}{2}$) frequency signal (Pfs = -20dBm) Versus input power Pin

A temporal simulation of frequency divider is done (Fig.5), according to this hypothesis. The output frequency being naturally half that of the input.

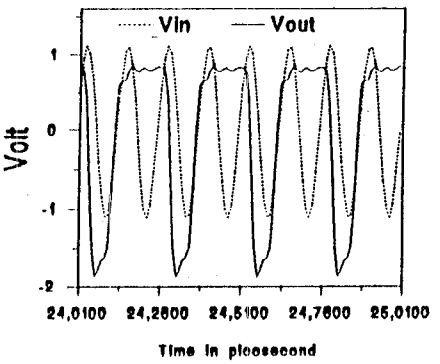

Fig.5 Input Vin and output Vout wave forme

3-EXPERIMENTAL RESULTS

It can be pointed out that the comparison between measured and simulated dc drain current (Fig.3) and nonlinear gain (Fig.4) of the MESFET, allows the autopolarisation to be validated.

The experimental frequency divider by 2 achieved is represented in Fig.6. Where

the combiner is a circulator. The phase shifter is produced by a variable length transmission line. The feed back relies on a 3dB power divider.

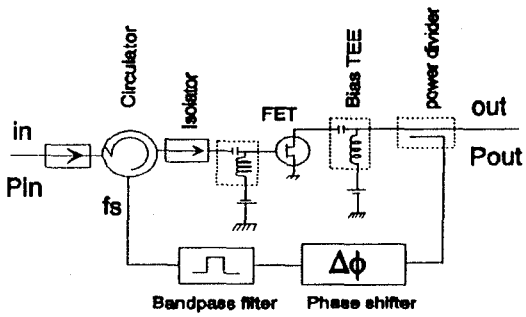

Fig.6 Experimental frequency divider by 2

The threshold input power measured is -4dBm. The maximum conversion gain is 10dB. And the present divider could operate on the (-5.0,+10dBm) power input range with conversion gain higher than 2dB. The output power versus input is given in Fig.7.

Note that the experimental and theoretical value of the conversion gain and the threshold input power are in good agreement.

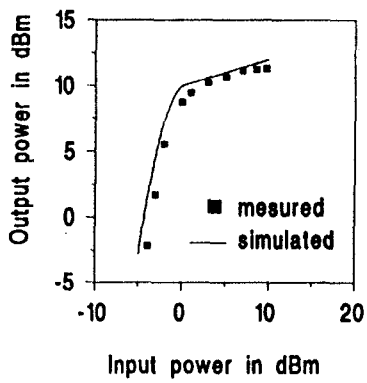

Fig.7 Output power versus input power

4-CONCLUSION

An original concept of frequency dividers based on the autopolarisation phenomenon has been proposed. This concept has been validated by analytic and simulation analysis.

Based on this concept an experimental frequency divider is produced, exhibiting high gain conversion and low threshold input power values. The good agreement between simulated and experimental results confirms our models and concept.

REFERENCES:

[1]S.V.AHAMED and all : 'study and fabrication of frequency divider-mulitiplier sheme for high effiency microwave power' IEEE Trans. Communication, pp 243-249, Feb 1976.

[2]R.L.MILLER: 'Fractional frequency generation utilizing regenerative modulation' Proc IRE,1939,37, pp 446-456 .

[3]G. IMMOVILLI and all : 'Analysis of a Miller frequency divider by tow in view of applications to wideband FM signals' Alta freq., 1973 , pp 313-323 .

[4]R.G. HARISSON : 'Theory of regeneratif frequency dividers using double balanced mixers'. IEEE on MTT symposium digest 1989, pp 459-462 .

[5]L.KIPNIS '20GHz frequency dividers silicon bipolar MMIC' Electronics letters Vol 23,24 sept 1987, No20, pp1085-1087.

[6]R.H. DERKSEN and all : '7.3 GHz Dynamic frequency dividers monolithically integred in a standard bipolar technology' IEEE on MTTT, vol36, pp537-541,MARCH 1988.

[7]K.KAZUHIKO: 'Novel approach for X-band GaAs Monolithic Analog 1/4 Frequency Divider' IEEE on MTT VOL 34, No4, april 1986, pp436-441.

[8]Y.TAJIMA and all : 'GaAsFET Large signal Model and its Application to circuit Designs', IEEE Trans. on ED, Vol.ED-28, No28, February1981.